NT7108

INTRODUCTION

The NT7108 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bit data latch, 64 bit drivers and decoder logic. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The NT7108 composed of the liquid crystal display system in combination with the NT7107.

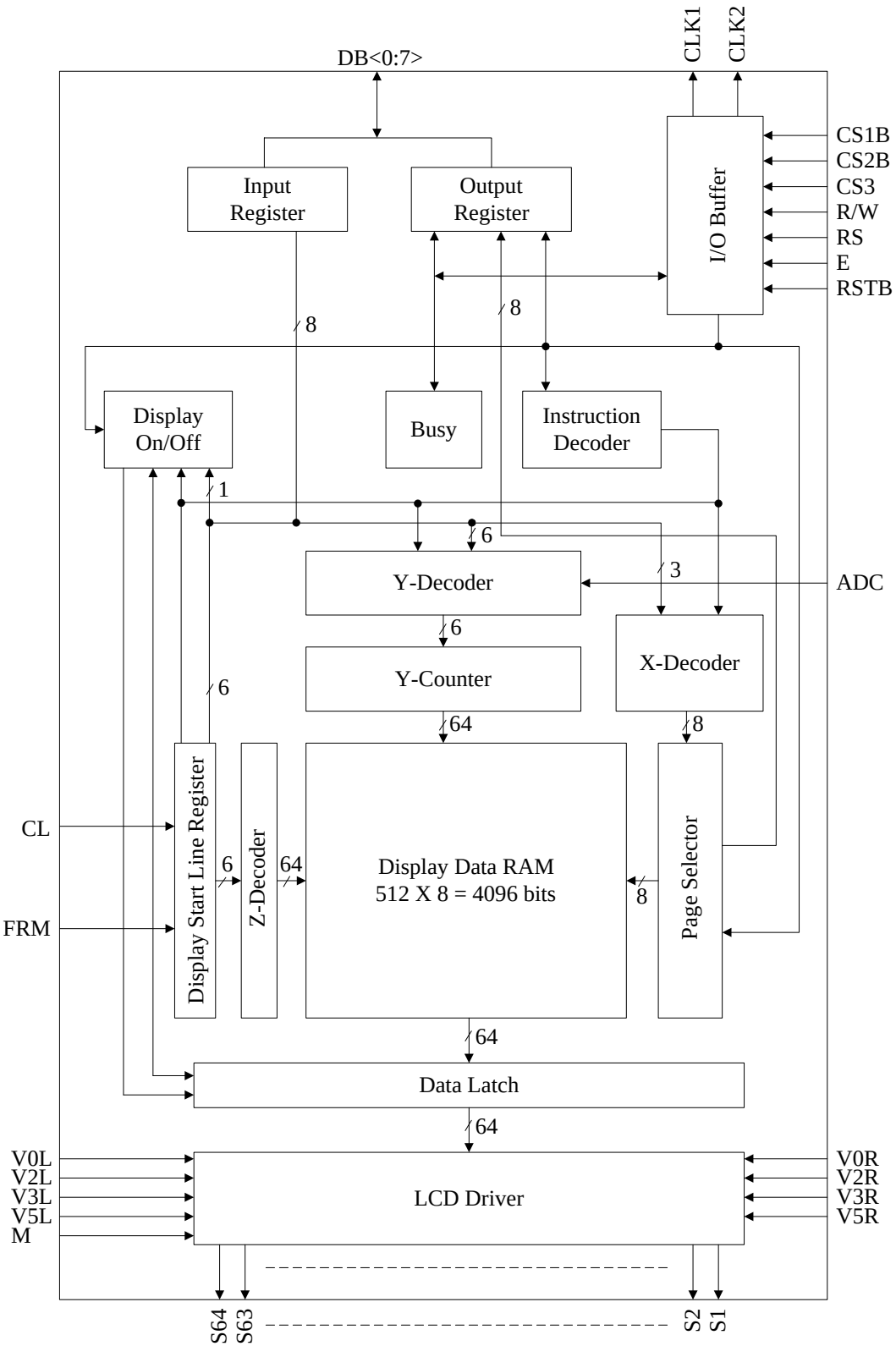
FEATURES

- Dot matrix LCD segment driver with 64 channel output
- Input and output signal
  - -Input: 8bit parallel display data control signal from MPU divided bias voltage (V0R, V0L, V2R, V2L, V3R, V3L, V5R, V5L)
  - -Output: 64 channel for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
  - -Capacity: 512 bytes (4096 bits)
  - -RAM bit data: RAM bit data = 1: On
    RAM bit data = 0: Off
- Applicable LCD duty:1/32-1/64
- LCD driving voltage: 8V-17V(V_{DD}-V_{EE})
- Power supply voltage:+2.7~+5.5V
- Interface

Driver		**Controller**
COMMON	SEGMENT	
Other NT7107	Other NT7108	MPU

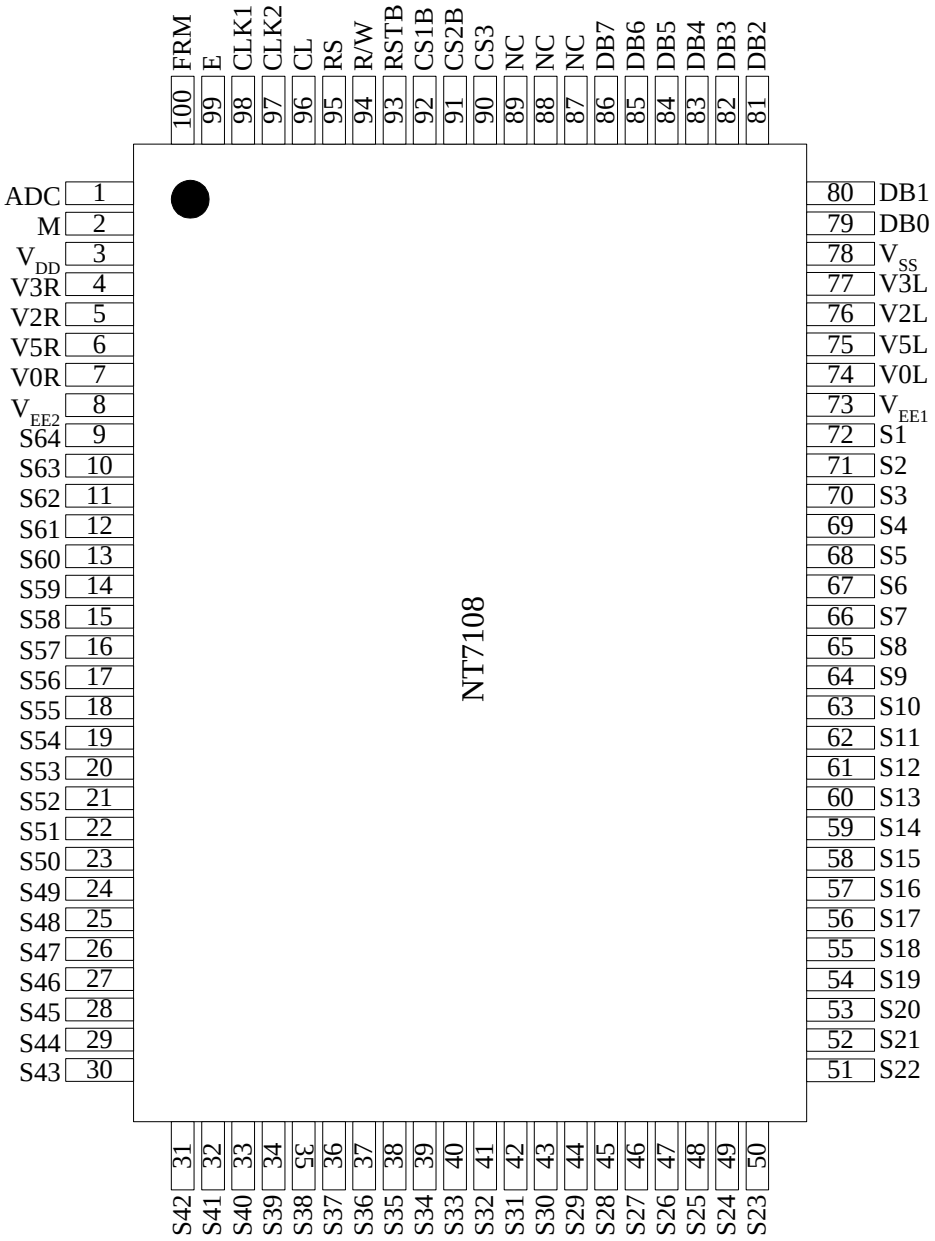
- High voltage CMOS process.
- 100QFP or bare chip available.

BLOCK DIAGRAM



PIN CONFIGURATION

100 QFP



PIN DESCRIPTION

Table 1. Pin Description

Pin Number QFP	Symbol	I/O	Description
3 78 73,8	V_{DD} V_{SS} $V_{EE1,2}$	Power	For internal logic circuit (+2.7~+5.5V) GND (0V) For LCD driver circuit VSS = 0V, V_{DD} = +5V±10%, V_{DD} - V_{EE} = 8V - 17V The same voltage should be connected to V_{EE1} and V_{EE2}.
74,7 76,5 77,4 75,6	V0L,V0R, V2L,V2R, V3L,V3R, V5L,V5R	Power	Bias supply voltage terminals to drive LCD. Select Level: V0L (R), V5L (R); Non-Select Level: V2L (R), V3L (R) The same voltage should connect V0L and V0R (V2L & V2R, V3L & V3R, V5L & V5R).
92 91 90	CS1B CS2B CS3	Input	Chip selection In order to interface data for input or output, the terminals have to be CS1B=L, CS2B=L, and CS3=H.
2	M	Input	Alternating signal input for LCD driving.
1	ADC	Input	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H Y0:S1-Y63:S64 ADC=L Y0:S64-Y63:S1
100	FRM	Input	Synchronous control signal. Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.
99	E	Input	Enable signal. Write mode (R/W=L)→ data of DB<0:7> is latched at the falling edge of E Read mode (R/W=H) → DB<0:7> appears the reading data while E is at high level.
98 97	CLK1 CLK2	Input	2 phase clock signal for internal operation Used to execute operations for input/output of display RAM data and others.
96	CL	Input	Display synchronous signal. Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.
95	RS	Input	Data or Instruction. RS=H → DB<0:7>:Display RAM data RS=L → DB<0:7>:Instruction data
94	RW	Input	Read or Write. R/W=H →Data appears at DB<0:7> and can be read by the CPU while E=H, CS1B=L, CS2B-L and CS3=H. R/W=L →Display data DB<0:7> can be written at falling of E when CS1B=L, CS2B=L and CS3=H.
79-86	DB0~ DB7	Input/ Output	Data bus. Three state I/O common terminal.

<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>72-9</td><td>S1-S64</td><td>Output</td><td>LCD segment driver output.
Display RAM data 1:On
Display RAM data 0:Off (relation of display RAM data & M)
<table>
<tr><th>M</th><th>Data</th><th>Output Level</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V2</td></tr>
<tr><td>H</td><td>V0</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V3</td></tr>
<tr><td>H</td><td>V5</td></tr>
</table></td></tr>
<tr><td>93</td><td>RSTB</td><td>Input</td><td>Reset signal.
When RSTB=L,
-ON/OFF register 0 set (display off)
-Display start line register 0 set (display line from 0)
After releasing reset, this condition can be changed only by instruction.</td></tr>
<tr><td>87
88
89</td><td>NC</td><td></td><td>No connection. (Open)</td></tr>
</table>

OPERATING PRINCIPLES AND METHODS

I/O BUFFER

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

INPUT REGISTER

Input register is provided to interface with MPU whose is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register, then into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

OUTPUT REGISTER

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

RESET

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

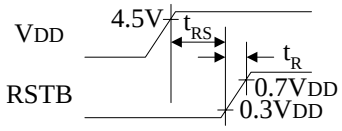
When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in table 1.

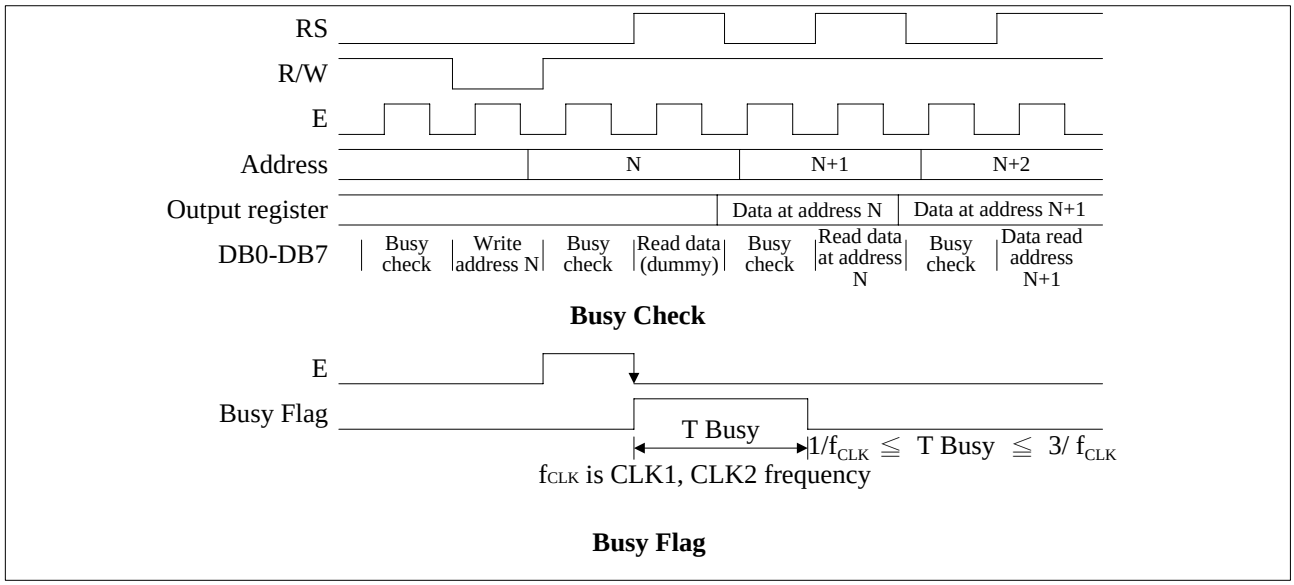
Table 2. Power Supply Initial Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	t_{RS}	1.0	-	-	μ s
Rise time	t_R	-	-	200	ns



Busy Flag

Busy Flag indicates the NT7108 is operating or no operating. When busy flag is high, NT7108 is in internal operating. When busy flag is low, NT7108 can accept the data or instruction. DB7 indicates busy flag of the NT7108.



Display ON / OFF Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non-selective voltage appears on segment output terminals. When flip-flop is set (logic high), non-selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segments disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

X Page Register

X page register designates pages of the internal display data RAM. Count function is not available. An address is set by instruction.

Y Address Counter

An Address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

- ADC=H →Y-address 0:S1-Y address 63:S64
- ADC=L → Y-address 0:S64-Y address 63:S1

ADC terminal connects the VDD or Vss.

Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.

DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the NT7108. Instruction is received from MPU to NT7108 for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set address (Y address)	L	L	L	H	Y address (0-63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0-7)			Sets the X address at the X address register.
Display Start line (Z address)	L	L	H	H	Display start line (0-63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On/ Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0: 7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0: 7) from display data RAM to the data bus.

DISPLAY ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

SET ADDRESS (Y ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0-AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

SET PAGE (X ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address (AC0-AC2) of the display data RAM is set in the X address register. Writing or reading to or from MPU is executed in this specified page until the next page is set.

DISPLAY START LINE (Z ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0-AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others (1/32-1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

STATUS READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY

  When BUSY is 1, the Chip is executing internal operation and o instructions are accepted.

  When BUSY is 0, the Chip is ready to accept any instructions.

- ON/OFF

  When ON/OFF is 1, the display is OFF.

  When ON/OFF is 0, the display is ON.

- RESET

  When RESET is 1, the system is being initialized.

  In this condition, no instructions except status read can be accepted.

  When RESET is 0, initializing has finished and the system is in usual operation condition.

WRITE DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0-D7) into the display data RAM. After writing instruction, Y address is increased by 1automatically.

READ DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0-D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	V_{DD}-19.0 to V_{DD} +0.3		(4)
Driver supply voltage	V_B	-0.3 to V_{DD} +0.3		(1),(3)
	V_{LCD}	V_{EE}-0.3 to V_{DD} +0.3		(2)
Operating temperature	T_{OPR}	-30 to +85	℃	
Storage temperature	T_{STG}	-55 to +125		

NOTES:

1. Based on Vss=0V
2. Applies the same supply voltage to V_{EE1} and V_{EE2}. V_{LCD}=V_{DD}-V_{EE}.
3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0-DB7.
4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).

Voltage level: $V_{DD} \geqq$ V0L=V0R $\geqq$ V2L=V2R $\geqq$ V3L=V3R $\geqq$ V5L=V5R $\geqq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=5.0V, Vss=0V, V_{DD}-V_{EE}=8 to 17V, Ta=-30℃ to +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{DD}	-	2.7	-	5.5	V	
Input high Voltage	V_{IH1}	-	0.7V_{DD}	-	V_{DD}		(1)
	V_{IH2}	-	2.0	-	V_{DD}		(2)
Input low Voltage	V_{IL1}	-	0	-	0.3V_{DD}		(1)
	V_{IL2}	-	0	-	0.8		(2)
Output high voltage	V_{OH}	I_{OH}=-200 μA	2.4	-	-		(3)
Output low voltage	V_{OL}	I_{OL}=1.6mA	-	-	0.4		(3)
Input leakage current	I_{LKG}	V_{IN}=V_{SS}-V_{DD}	-1.0	-	1.0	μA	(4)
Three-state(off) input current	I_{TSL}	V_{IN}=V_{SS}-V_{DD}	-5.0	-	5.0		(5)
Driver input leakage current	I_{DIL}	V_{IN}=V_{EE}-V_{DD}	-2.0	-	2.0		(6)
Operating current	I_{DD1}	During display	-	-	100		(7)
	I_{DD2}	During access Access cycle = 1 MHz	-	-	500		(7)
On resistance	R_{ON}	V_{DD}-V_{EE}=15V I_{LOAD}= ±0.1mA	-	-	7.5	kΩ	(8)

NOTES:

1. CL, FRM, M RSTB, CLK1, CLK2
2. CS1B, CS2B, CS3, E, R/W, RS, DB0 - DB7
3. DB0 - DB7
4. Except DB0 -DB7
5. DB0 - DB7 at high impedance
6. V0L(R), V2L(R), V3L(R), V5L(R)
7. 1/64 duty, f_{CLK}=250kHz, frame frequency=70HZ, output: no load
8. VDD - VEE =15.5V

V0L(R)>V2L(R)=V_{DD}-2/7(V_{DD}-V_{EE})>V3L(R)=V_{EE}+2/7(V_{DD}-V_{EE})>V5L(R)

AC CHARACTERISTICS (V_{DD}=+5V±10%, Vss=0V, Ta=-30℃ to +85℃)

Clock Timing

Characteristic	Symbol	Min	Type	Max	Unit
CLK1, CLK2 cycle time	t_{CY}	2.5	-	20	μs
CLK1 "low" level width	t_{WL1}	625	-	-	ns
CLK2 "low" level width	t_{WL2}	625	-	-	
CLK1 "high" level width	t_{WH1}	1875	-	-	
CLK2 "high" level width	t_{WH2}	1875	-	-	
CLK1-CLK2 phase difference	t_{D12}	625	-	-	
CLK2-CLK1 phase difference	t_{D21}	625	-	-	
CLK1, CLK2 rise time	t_R	-	-	150	
CLK1, CLK2 fall time	t_F	-	-	150	

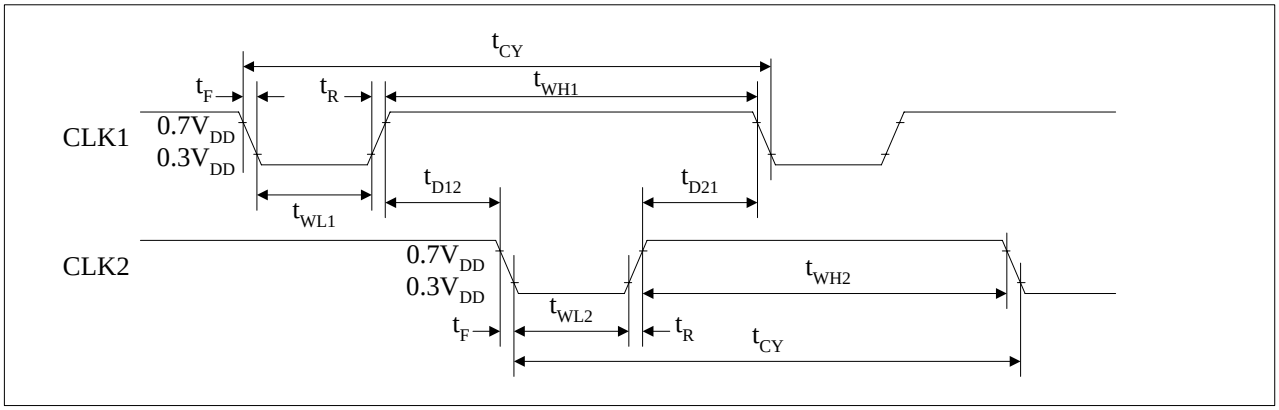


Figure 1. External Clock Waveform

Display Control Timing

Characteristic	Symbol	Min	Type	Max	Unit
FRM delay time	t_{DF}	-2	-	2	μs
M delay time	t_{DM}	-2	-	2	
CL "low" level width	t_{WL}	35	-	-	
CL "high" level width	t_{WH}	35	-	-	

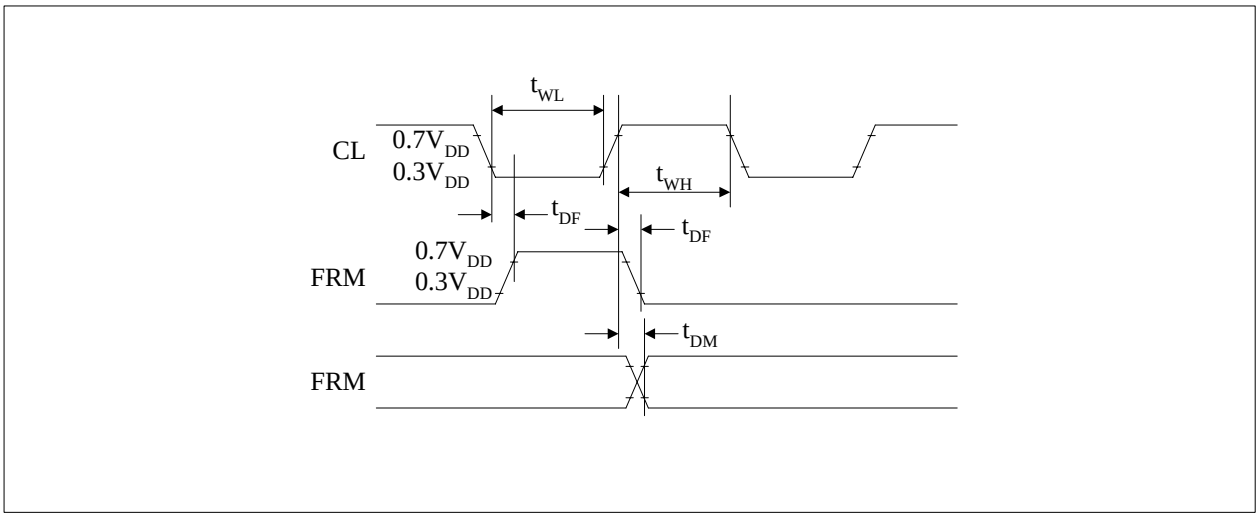


Figure 2. Display Control Waveform

MPU Interface

Characteristic	Symbol	Min	Type	Max	Unit
E cycle	t_C	1000	-	-	ns
E high level width	t_{WH}	450	-	-	
E low level width	t_{WL}	450	-	-	
E rise time	t_R	-	-	25	
E fall time	t_F	-	-	25	
Address set-up time	t_{ASU}	140	-	-	
Address hold time	t_{AH}	10	-	-	
Data set-up time	t_{DSU}	200	-	-	
Data delay time	t_D	-	-	320	
Data hold time (write)	t_{DHW}	10	-	-	
Data hold time (read)	t_{DHR}	20	-	-	

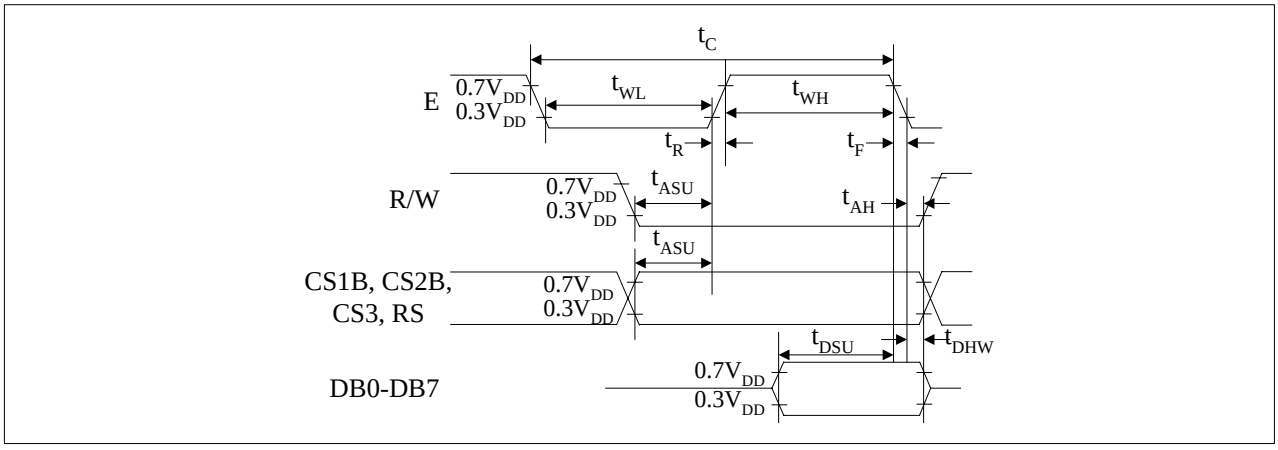


Figure 3. MPU Write Timing

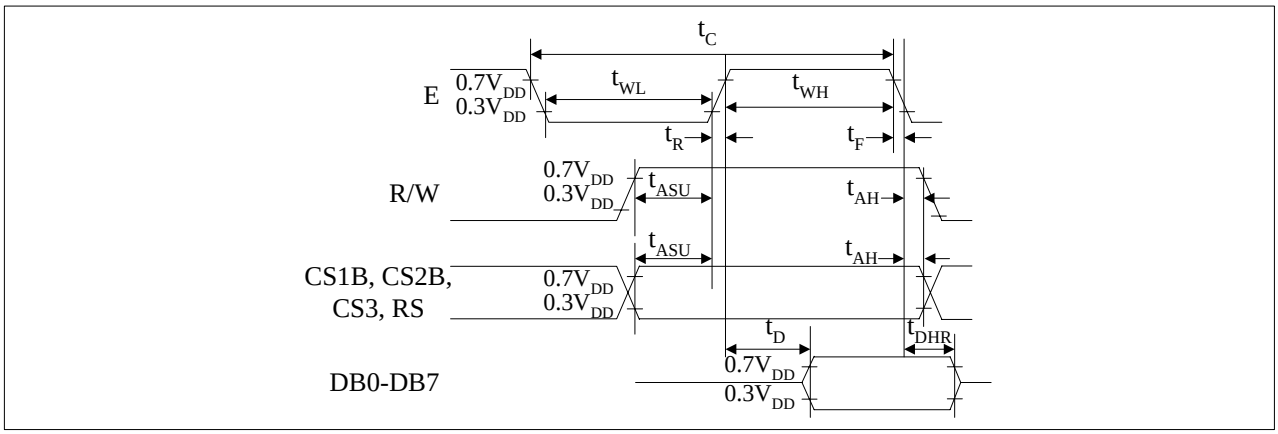
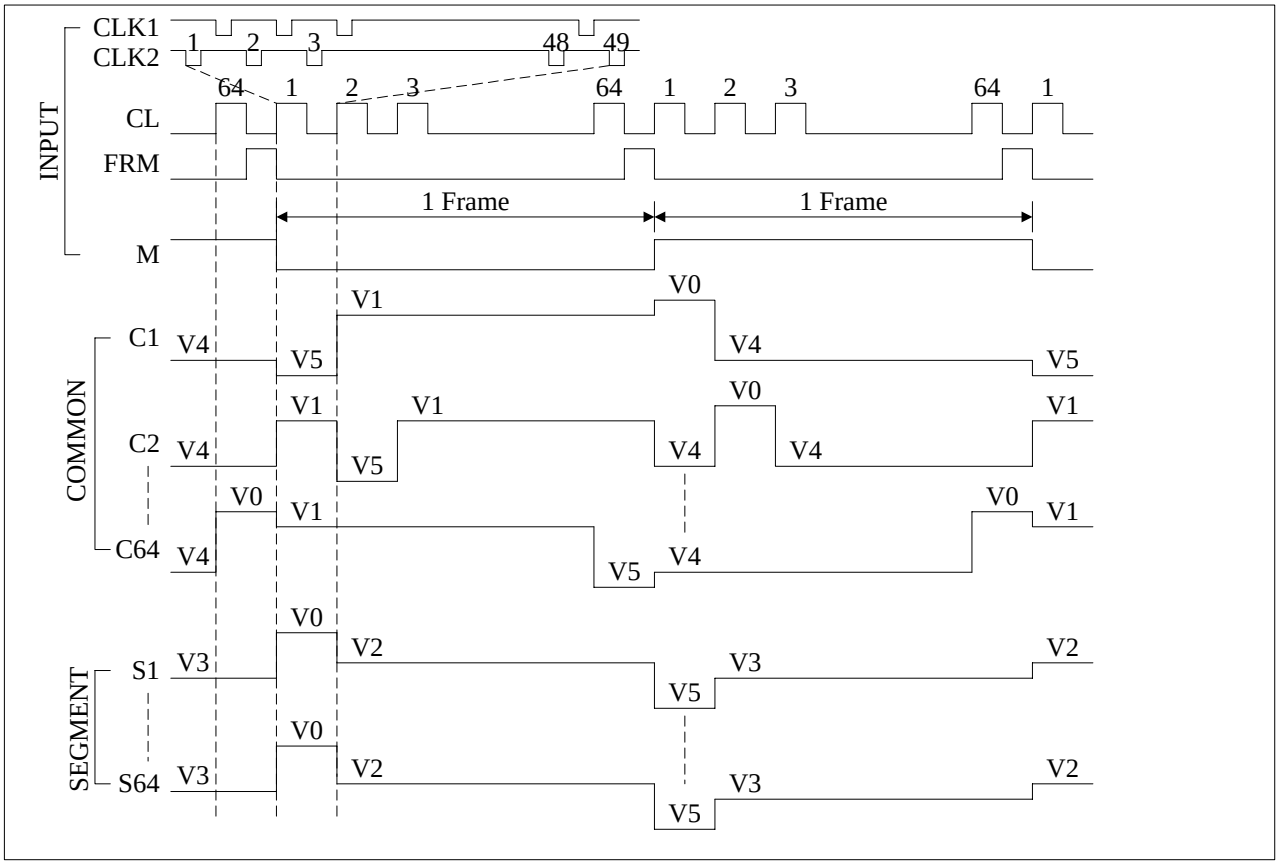


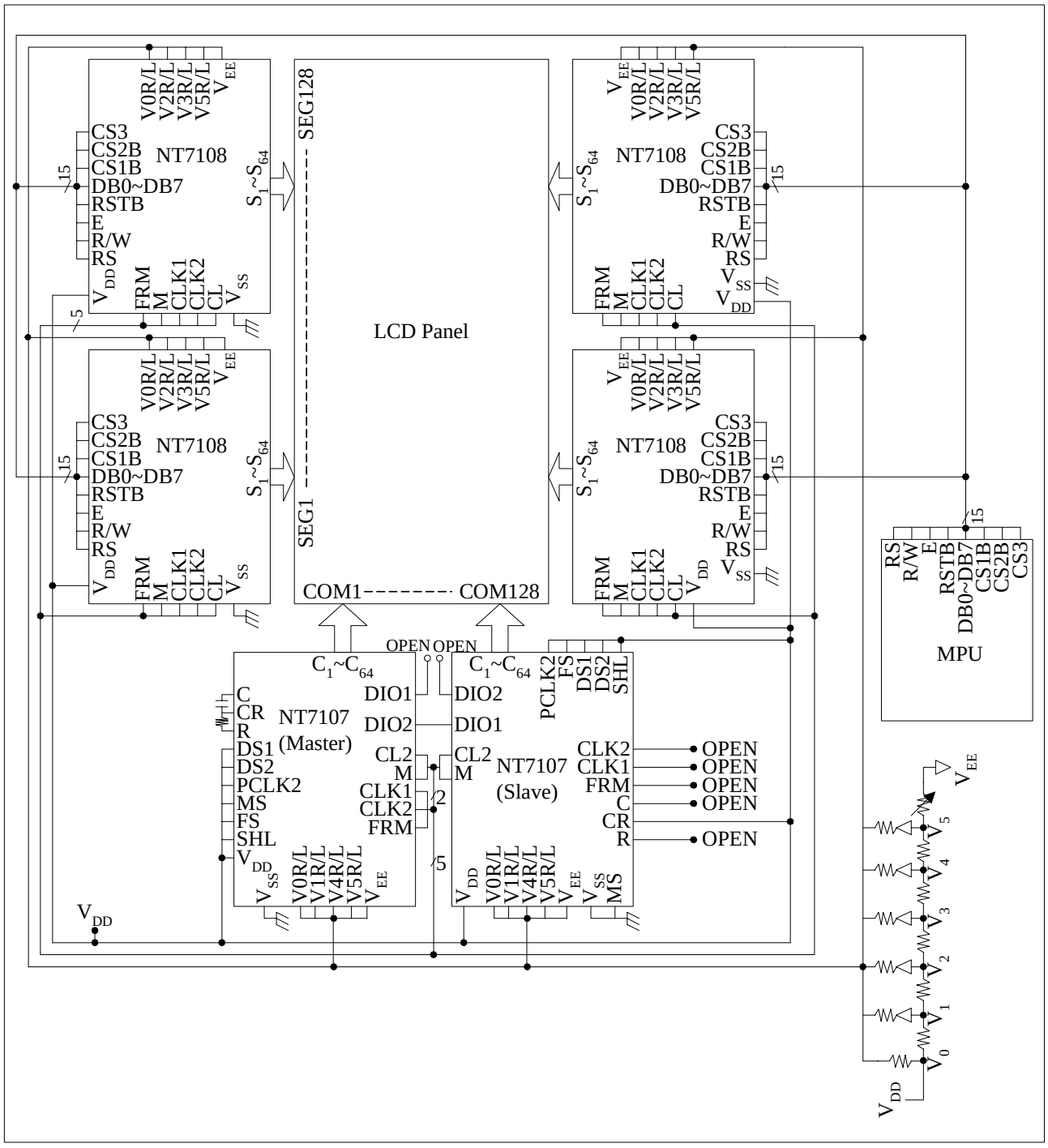
Figure 4. MPU Read Timing

TIMING DIAGRAM (1/64 DUTY)



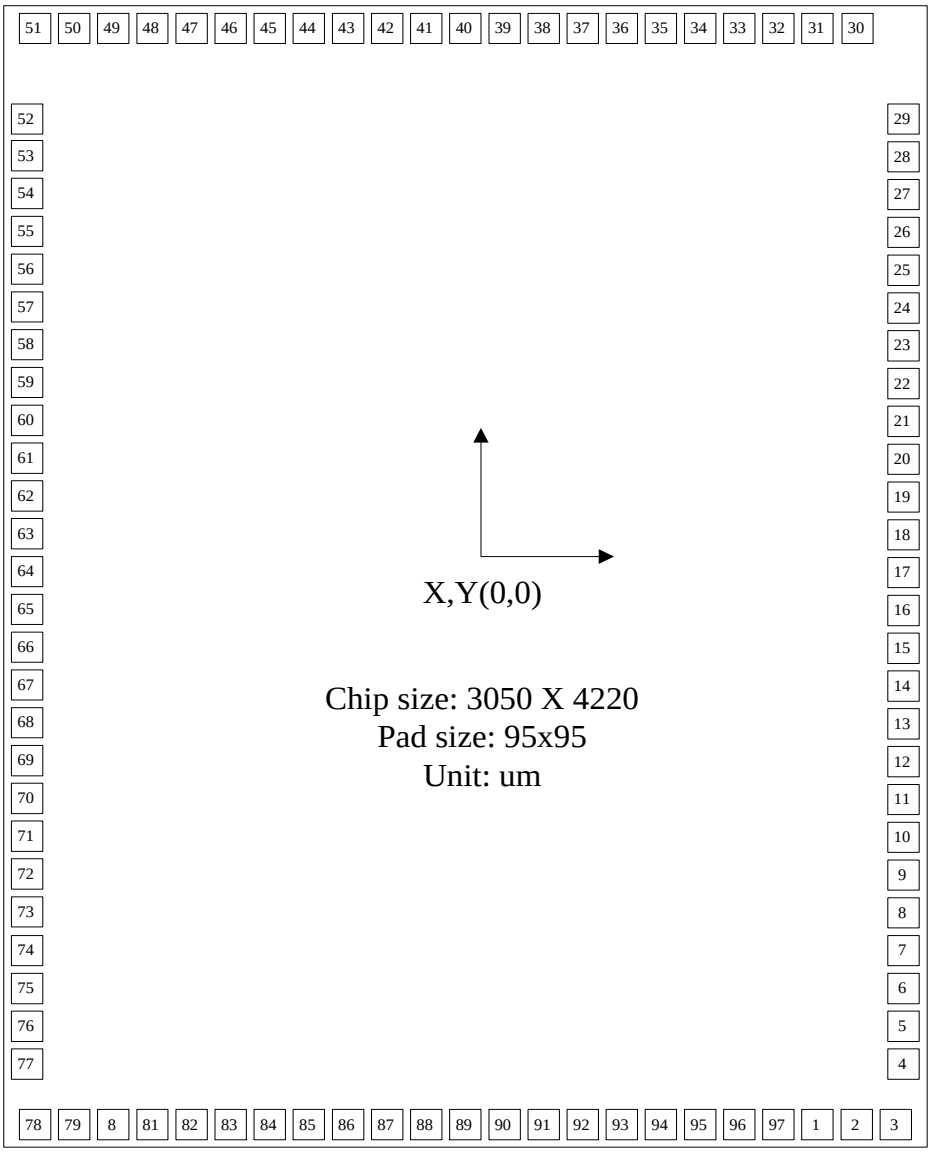
APPLICATION CIRCUIT

1/128 duty COMMON driver (NT7107) interface circuit



PAD DIAGRAM

Note: Please connects the substrate to V_{DD} or floating



PAD DIAGRAM

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	ADC	1125.000	-1994.198	50	SEG23	-1187.500	1994.200
2	M	1250.000	-1994.198	51	SEG22	-1312.500	1994.200
3	VDD	1375.000	-1994.198	52	SEG21	-1408.098	1399.700
4	V3R	1408.100	-1725.300	53	SEG20		1274.700
5	V2R		-1600.300	54	SEG19		1149.700
6	V5R		-1475.300	55	SEG18		1024.700
7	V0R		-1350.300	56	SEG17		899.700
8	VEE		-1225.300	57	SEG16		774.700
9	SEG64		-1100.300	58	SEG15		649.700
10	SEG63		-975.300	59	SEG14		524.700
11	SEG62		-850.300	60	SEG13		399.700
12	SEG61		-725.300	61	SEG12		274.700
13	SEG60		-600.300	62	SEG11		149.700
14	SEG59		-475.300	63	SEG10		27.700
15	SEG58		-350.300	64	SEG9		-100.300
16	SEG57		-225.300	65	SEG8		-225.300
17	SEG56		-100.300	66	SEG7		-350.300
18	SEG55		24.700	67	SEG6		-475.300
19	SEG54		149.700	68	SEG5		-600.300
20	SEG53		274.700	69	SEG4		-725.300
21	SEG52		399.700	70	SEG3		-850.300
22	SEG51		524.700	71	SEG2		-975.300
23	SEG50		649.700	72	SEG1		-1100.300
24	SEG49		774.700	73	VEE		-1225.300
25	SEG48		899.700	74	V0L		-1350.300
26	SEG47		1024.700	75	V5L		-1475.300
27	SEG46		1124.700	76	V2L		-1600.300
28	SEG45		1274.700	77	V3L		-1725.300
29	SEG44		1399.700	78	GND	-1375.000	-1994.198
30	SEG43	1312.500	1994.200	79	DB0	-1250.000	
31	SEG42	1187.500		80	DB1	-1125.000	
32	SEG41	1062.500		81	DB2	-1000.000	
33	SEG40	937.500		82	DB3	-875.000	
34	SEG39	812.500		83	DB4	-750.000	
35	SEG38	687.500		84	DB5	-625.000	
36	SEG37	562.500		85	DB6	-500.000	
37	SEG36	437.500		86	DB7	-375.000	
38	SEG35	312.500		87	CS3	-250.000	
39	SEG34	187.500		88	CS2B	-125.000	
40	SEG33	62.500		89	CS1B	0.000	
41	SEG32	-62.500		90	RSTB	125.000	
42	SEG31	-187.500		91	R/W	250.000	
43	SEG30	-312.500		92	RS	375.000	
44	SEG29	-437.500		93	CL	500.000	
45	SEG28	-562.500		94	CLK2	625.000	
46	SEG27	-687.500		95	CLK1	750.000	
47	SEG26	-812.500		96	E	875.000	
48	SEG25	-937.500		97	FRM	1000.000	
49	SEG24	-1062.500					

VERSION HISTORY

Date	Description
6/5/2002	Add the notice of substrate connection.
12/11/2002	To correct some mistakes at page 5,6,15,19